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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/436,984	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,31-55 and 60-83* is/are pending in the application.

4a) Of the above claim(s) *1-14 and 31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-55 and 60-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

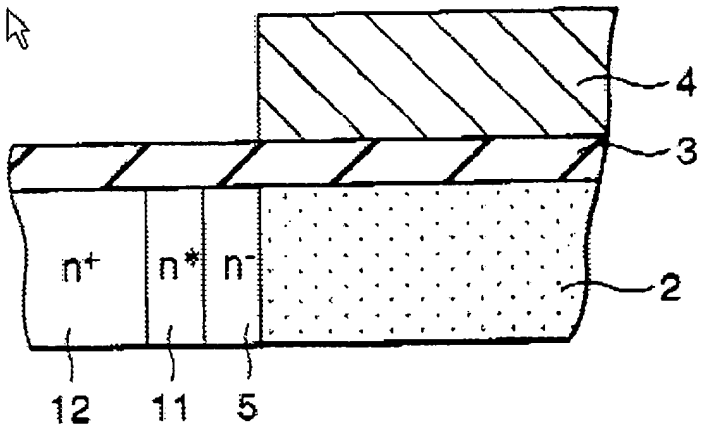
1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).



3. Claims 32-55 and 60-83 are rejected under 35 U.S.C. 102(e) as being anticipated by Kamiura et al., U.S. Patent 6,288,413 B1.

4. Kamiura discloses a semiconductor devices as claimed. See **FIGS. 1A-9**.

Pertaining to claim 32, Kamiura teaches a semiconductor device comprising:

a semiconductor film **20** formed on an insulating surface **1**;

a channel forming region **2** in the semiconductor film;

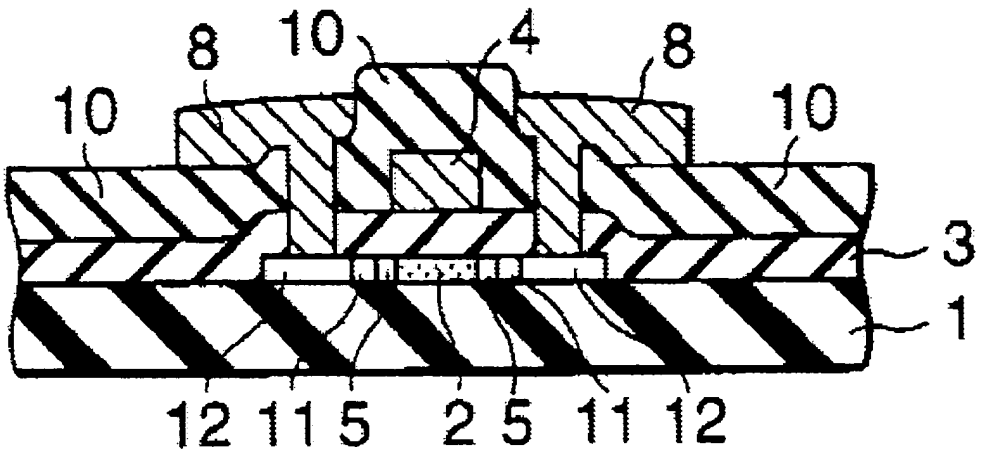
a gate insulating film **3** formed on the semiconductor film;

a gate electrode **4** formed over the channel forming region **2** with the gate insulating film interposed therebetween; a pair of side walls **6b** adjacent to side surfaces of the gate electrode **4**;

a pair of first impurity regions **5** doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls overlap the pair of first impurity regions; and

a pair of second impurity regions **11** doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions **12** doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions, wherein the pair of side walls do not overlap the pair of second impurity regions and third impurity regions.



5. Pertaining to claim 33, Kamiura teaches the semiconductor device according to claim 32 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

6. Pertaining to claim 34, Kamiura teaches the semiconductor device according to claim 32 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

7. Pertaining to claim 35, Kamiura teaches the semiconductor device according to claim 32 wherein the side walls comprise silicon **4**.

8. Pertaining to claim 36, Kamiura teaches the semiconductor device according to claim 32 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor (column , line 16).

9. Pertaining to claim 38, Kamiura teaches a semiconductor device comprising: a semiconductor film formed on an insulating surface; a channel forming region in the semiconductor film;

a gate insulating film formed on the semiconductor film;

a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween;

a pair of conductive side walls adjacent to side surfaces of the gate electrode;

a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls overlap the pair of first impurity regions; and

a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions, wherein the pair of side walls do not overlap the pair of second impurity regions and third impurity regions.

10. Pertaining to claim 39, Kamiura teaches the semiconductor device according to claim 38 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

11. Pertaining to claim 40, Kamiura teaches the semiconductor device according to claim 38 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

12. Pertaining to claim 41, Kamiura teaches the semiconductor device according to claim 38 wherein the side walls comprise silicon.

13. Pertaining to claim 42, Kamiura teaches the semiconductor device according to claim 38 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

14. Pertaining to claim 44, Kamiura teaches a semiconductor device comprising:

(a) a thin film transistor over a substrate, said thin film transistor comprising: a semiconductor film formed on an insulating surface; a channel forming region in the semiconductor film; a gate insulating film formed on the semiconductor film; a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween; a pair of side walls adjacent to side surfaces of the gate electrode; a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls overlap the pair of first impurity regions; and a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions; wherein the pair of side walls do not overlap the pair of second impurity regions and third impurity regions;

(b) an interlayer insulating film formed over the thin film transistor; and

for element (c) a pixel electrode formed over the interlayer insulating film and electrically connected to one of the third impurity regions.

15. Pertaining to claim 45, Kamiura teaches the semiconductor device according to claim 44 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

16. Pertaining to claim 46, Kamiura teaches the semiconductor device according to claim 44 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

17. Pertaining to claim 47, Kamiura teaches the semiconductor device according to claim 44 wherein the side walls comprise silicon.

18. Pertaining to claim 48, Kamiura teaches the semiconductor device according to claim 44 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

19. Pertaining to claim 50, Kamiura teaches a semiconductor device comprising:

(a) a thin film transistor formed over a substrate, said thin film transistor comprising: a semiconductor film formed on an insulating surface; a channel forming region in the semiconductor film; a gate insulating film formed on the semiconductor film; a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween; a pair of conductive side walls adjacent to side surfaces of the gate electrode; a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls overlap the pair of first impurity regions; and a pair of second impurity regions doped

with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions; wherein the pair of side walls do not overlap the pair of second impurity regions and third impurity regions;

(b) an interlayer insulating film formed over the thin film transistor; and

(c) a pixel electrode formed over the interlayer insulating film and electrically connected to one of the third impurity regions.

20. Pertaining to claim 51, Kamiura teaches the semiconductor device according to claim 50 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

21. Pertaining to claim 52, Kamiura teaches the semiconductor device according to claim 50 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

22. Pertaining to claim 53, Kamiura teaches the semiconductor device according to claim 50 wherein the side walls comprise silicon.

23. Pertaining to claim 54, Kamiura teaches the semiconductor device according to claim 50 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

24. Pertaining to claim 60, Kamiura teaches a semiconductor device comprising:

a semiconductor film formed on an insulating surface;

a channel forming region in the semiconductor film;

a gate insulating film formed on the semiconductor film;

a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween; .

a second insulating film in contact with an upper surface and side surfaces of the gate electrode;

a pair of side walls adjacent to the side surfaces of the gate electrode with the second insulating film interposed therebetween;

a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions; and

a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions, wherein the pair of side walls do not overlap the pair the pair of second impurity regions and third impurity regions.

25. Pertaining to claim 61, Kamiura teaches the semiconductor device according to claim 60 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

26. Pertaining to claim 62, Kamiura teaches the semiconductor device according to claim 60 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

27. Pertaining to claim 63, Kamiura teaches the semiconductor device according to claim 60 wherein the side walls comprise silicon.

28. Pertaining to claim 64, Kamiura teaches the semiconductor device according to claim 60 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

29. Pertaining to claim 66, Kamiura teaches a semiconductor device comprising:
(a) a thin film transistor over a substrate, said thin film transistor comprising:
a semiconductor film formed on an insulating surface;
a channel forming region in the semiconductor film; a gate insulating film formed on the semiconductor film; a gate electrode formed over the channel forming region with the gate insulating film interposed therebetween;
a second insulating film in contact with an upper surface and side surfaces of the gate electrode;
a pair of side walls adjacent to the side surfaces of the gate electrode with the second insulating film interposed therebetween;

a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the semiconductor film with the channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions; and a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the semiconductor film adjacent to the pair of first impurity regions; and

a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the semiconductor film with the pair of second impurity regions extending between the channel forming region and the pair of third impurity regions, wherein the pair of side walls do not overlap the pair the pair of second impurity regions and third impurity regions.

(b) an interlayer insulating film formed over the thin film transistor; and

(c) a pixel electrode formed over the interlayer insulating film and electrically connected to one of the third impurity regions.

30. Pertaining to claim 67, Kamiura teaches the semiconductor device according to claim 66 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

31. Pertaining to claim 68, Kamiura teaches the semiconductor device according to claim 66 wherein the N-type impurity added in the first, second arid third impurity regions comprises phosphorous.

32. Pertaining to claim 69, Kamiura teaches the semiconductor device according to claim 66 wherein the side walls comprise silicon.

33. Pertaining to claim 70, Kamiura teaches the semiconductor device according to claim 66 wherein the semiconductor device is one selected from a liquid crystal display device, an El. display device and an image sensor.

34. Pertaining to claim 72, Kamiura teaches a semiconductor device comprising a CMOS circuit comprising:

an NTFT having: a first semiconductor film formed on an insulating surface;

a first channel forming region in the first semiconductor film; a first gate insulating film formed on the first semiconductor film;

a first gate electrode formed over the first channel forming region with the first gate insulating film interposed therebetween;

a pair of side walls adjacent to side surfaces of the first gate electrode; a second insulating film on the first gate electrode and the pair of side walls; and

a PTFT having a second semiconductor film formed on an insulating surface; a second channel forming region in the second semiconductor film (i.e., CMOS, column 2, line 63);

a third gate insulating film formed on the second semiconductor film;

a second gate electrode formed over the second channel forming region with the third gate insulating film interposed therebetween;

wherein a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the first semiconductor film with the first channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions;

wherein a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first: concentration and formed in the first semiconductor film adjacent to the pair of first impurity regions; and

wherein a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the first semiconductor film with the pair of second impurity regions extending between the first channel forming region and the pair of third impurity regions, wherein the pair of side walls do not overlap the pair the pair of second impurity regions and third impurity regions.

35. Pertaining to claim 73, Kamiura teaches the semiconductor device according to claim 72 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

36. Pertaining to claim 74, Kamiura teaches the semiconductor device according to claim 72 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

37. Pertaining to claim 75, Kamiura teaches the semiconductor device according to claim 72 wherein the side walls comprise silicon.

38. Pertaining to claim 76, Kamiura teaches the semiconductor device according to claim 72 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

39. Pertaining to claim 78, Kamiura teaches a semiconductor device comprising a CMOS circuit comprising:

an NTFT having: a first semiconductor film formed on an insulating surface;

a first channel forming region in the first semiconductor film; a first gate insulating film formed on the first semiconductor film;

a first gate electrode formed over the first channel forming region with the first gate insulating film interposed therebetween;

a second insulating film in contact with an upper surface and side surfaces of the first gate electrode;

a pair of side walls adjacent to the side surfaces of the first gate electrode with the second insulating film interposed therebetween; and

a PTFT having: a second semiconductor film formed on an insulating surface; a second channel forming region in the second semiconductor film (i.e., CMOS column 2, line 63);

a third gate insulating film formed on the second semiconductor film;

a second gate electrode formed over the second channel forming region with the third gate insulating film interposed therebetween;

wherein a pair of first impurity regions doped with an N-type impurity at a first concentration and formed in the first semiconductor film with the first channel forming region extending therebetween wherein the pair of side walls only overlap the pair of first impurity regions;

wherein a pair of second impurity regions doped with an N-type impurity at a second concentration greater than the first concentration and formed in the first semiconductor film adjacent to the pair of first impurity regions; and

wherein a pair of third impurity regions doped with an N-type impurity at a third concentration greater than the second concentration and formed in the first semiconductor film with the pair of second impurity regions extending between the first channel forming region and the pair of third impurity regions, wherein the pair of side walls do not overlap the pair the pair of second impurity regions and third impurity regions.

40. Pertaining to claim 79, Kamiura teaches the semiconductor device according to claim 78 wherein the N-type impurity added in the first, second and third impurity regions comprises an element selected from the group 15 elements.

41. Pertaining to claim 80, Kamiura teaches the semiconductor device according to claim 78 wherein the N-type impurity added in the first, second and third impurity regions comprises phosphorous.

42. Pertaining to claim 81, Kamiura teaches the semiconductor device according to claim 78 wherein the side walls comprise silicon.

43. Pertaining to claim 82, Kamiura teaches the semiconductor device according to claim 78 wherein the semiconductor device is one selected from a liquid crystal display device, an EL display device and an image sensor.

44. Pertaining to claims 37, 43, 49, 55, 65, 71, 77 and 83, Kamiura discloses a semiconductor device is one selected from a video camera, a digital camera, a projector, a goggle type display, a car navigation device, a personal computer and a portable information terminal (column 1, lines 14-19).

Claims 32-55 and 60-83 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al., U.S. Patent 5,789,762.

Conclusion

45. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

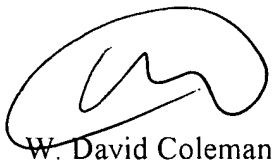
46. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

47. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

48. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

49. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. David Coleman
Primary Examiner
Art Unit 2823

WDC